

**Amendments to the Specification**

**Please replace the paragraph beginning on page 1, line 9 through line 14 with the following amended paragraph:**

A1  
Conventionally, to prepare a speed pattern in a positioning device (CPU, controllers, servo amplifiers, and the like), the speed pattern preparation cycle and speed data are set as shown in Figs. 3 3(a) and 3(b), that is, speed data is set to 32 bits in both Fig. 3(a) and Fig. 3(b), and by means of the fixed decimal mode, 16 bits are set for the integer part and 16 bits are set for the decimal part to fix the decimal point position. The speed pattern preparation cycle as a cycle for outputting speed data is set to 8m sec in the case of Fig. 3(a) and 64m sec in the case of Fig. 3(b).

Please replace the paragraph beginning on page 6, line 6 through line 10 with the following amended paragraph:

A2  
The speed pattern preparation unit 1 calculates a speed pattern based on the inputted speed pattern preparation cycle 3 and moving instruction (moving distance and acceleration and deceleration time) 2, and the size of the computing range in this case is set to have a fixed length inside the positioning device. In this computing range with a fixed length, as shown in Figs. 2 2(a) and 2(b) show ~~an example~~ examples in which the speed data size is 32 bits.